Application Note – AN101

Considerations for Measurement of PCR Jitter

H. Pandya

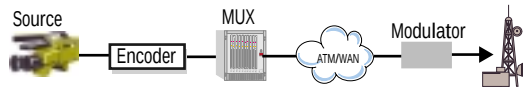
Sr. Design Engineer, Pixelmetrix Corporation

PCR, or Program Clock Reference, is fundamental to the timing recovery mechanism for MPEG2 transport streams. PCR values are embedded into the adaptation field within the transport packets of defined PIDs.

This document describes the method employed in the DVStation for the real time measurement of irregularities in PCR signals of MPEG-2 Transport Streams.

Introduction to PCR Jitter

Moving video images must be delivered in real time and with a consistent rate of presentation in order to preserve the illusion of motion. However, delays introduced by coding, multiplexing and transmission can cause a variable amount of delay for video packets arriving at the decoder. This delay wrecks havoc in the decoding process mandating buffers in the decoder.



The MPEG-2 standard provides an additional mechanism to ensure video frames can be decoded and delivered to the viewer with a consistent rate of display – that mechanism is called the Program Clock Reference.

PCR, or Program Clock Reference, is fundamental to the timing recovery mechanism for MPEG2 transport streams. PCR values are embedded into the adaptation field within the transport packets of defined PIDs. PCR consists of two parts totaling 42-bits. The PCR values increment with a standard clock rate of 27 MHz. PCR values roll over roughly once in a day.

As PCR is used by the IRDs to derive the clock reference, any jitter or drift in the PCR clock can have damaging effect on the IRD's performance.

The irregularities in the PCR can be broadly classified into jitter and offset.

Jitter in the PCR is mainly attributed to two sources: systematic jitter (or PCR accuracy error, PCR_AC), and network jitter. Systematic jitter and network jitter are combined to get overall jitter (PCR_OJ).

Systematic jitter arises primarily because of the repetition rate of the transport stream packets on the PID containing PCR not being a multiple of the PCR clock time. Apart from this, other systematic malfunctions along the transport chain may also result in PCR jitter. Improper management of input and output data rates on the transport buffers is another possible cause of PCR jitter. Network jitter is a result of variations in the propagation delay in the transmission path. Network jitter is also referred to as PCR_Arrival_time_jitter.

PCR offset is the difference of the PCR clock from the required clock rate of 27 MHz.

DVStation Timing Architecture

A TSP (Transport Stream Processor) card connects to one of the 21 slots of DVStation back-plane. Cards in each of the 21 slots of DVStation back-plane share a common high-accuracy reference clock. This clock can be derived from one of the user-selectable clock sources, including GPS, DVStation internal high-accuracy clock source, and SMPTE 259 clock source.

The TSP card generates a high-accuracy 108 MHz clock synchronized to the backplane clock source. The PCR timestamps on the received transport stream are compared with this local clock reference to measure the jitter. Since the reference clock (108 MHz) is an integral multiple of the PCR clock (27 MHz) any truncation and round-off errors in PCR jitter measurements are eliminated thus enhancing the accuracy of the measurement.

PCR Jitter Measurements

DVStation classifies the PCR jitter into two categories based on the frequency of variation.

The first category, PCR jitter, corresponds to short term variations with frequency more than 1 Hz. DVStation internally combines the jitter components PCR_AC and network jitter. The measurements shown by the DVStation represent PCR overall jitter, or PCR_OJ. This applies to PCR jitter histogram and the measurements of min and max jitter.

Each reading of the PCR jitter histogram is the difference between the instantaneous value of the PCR in the transport packet, and the timestamp of the drift-compensated reference clock. The drift compensation is a digital high-pass filter, which removes the effect of low frequency variation from the jitter values. The PCR jitter readings thus obtained are also used for computing minimum and maximum jitter.

The second category, PCR offset, measures long term variation between the frequency of the PCR clock and the reference clock. DVStation employs a digital low-pass filter with cut-off frequency of 10 milli-Hertz for computing PCR offset. PCR offset is measured in ppm.

Comparison with TR 101 290 Recommendations

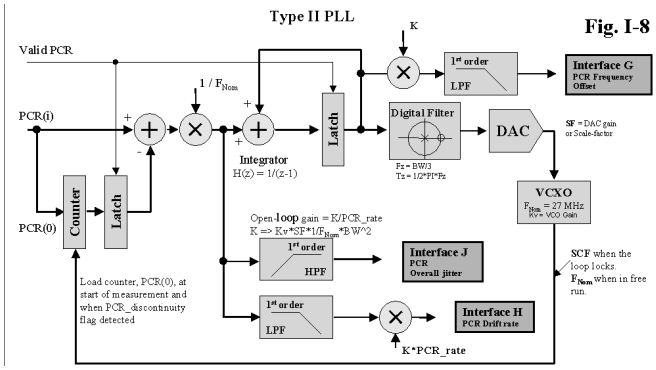
The PCR jitter measurement in the DVStation largely complies with the recommendations of the standard TR 101 290, with the following exceptions:

1. There is some difference between the DVStation's PCR measurement and the block diagram shown in Fig. I-8 in TR 101 290 (shown below). In Fig I-8, the reference clock (stated as VCXO) takes feedback from DAC, whose output is partly derived from filtered PCR values in the transport stream.

   In DVStation, the reference clock is completely independent of the PCR values in the transport stream. The Timing Reference Module (TRM) in the DVStation has a dedicated unit to ensure the stability of the reference clock. This way, DVStation is able to provide a stable, and completely independent reference clock for accurate PCR measurements.

2. DVStation internally consolidates PCR_AC and PCR_Arrival_time_jitter to compute PCR_OJ. Thus, the only PCR jitter measurement presented on the user interface is PCR_OJ.

3. The drift rate (PCR_DR) is not directly available. One can easily derive the drift rate with the post processing on the periodic log of PCR offset values. One of the easiest approaches will be to plot PCR offset against time.



TR101 290 Figure I-8

References

"Measurement Guidelines for DVB Systems", Draft TR 101 290, DVB.

REF : PPN30026

About DVStation

Pixelmetrix has focused on creating a single self-contained monitoring station that can analyze thousands of parameters within hundreds of digital television signals. Through the use of plug-in modules and parallel processing, we monitor all these parameters in real time, simultaneously and continuously. We've targeted our development efforts to insure the quality of the signal, the integrity of the program service and the delivery of essential technical information to the right people in a timely and meaningful manner.

Plug-in modules allow flexibility and accommodate changes in a fast evolving technical infrastructure. So far, we've focused on three categories of plug-in modules: physical line interfaces (ASI, SPI, RF, ATM etc.); a transport stream processor (TSP); and picture quality processors.

In our design, a line interface module extracts the MPEG-2 transport stream from the native RF or telecom signals and passes that data to a TSP – Transport Stream Processor. Line interface modules provide monitoring capability on the physical layer. For RF interfaces (QPSK, QAM, COFDM, 8VSB, etc.) monitoring means to check carrier level, C/N (carrier-to-noise ratio), bit error rate and EVM (Error Vector Magnitude), or other parameters that may be applicable. Additionally, a simple constellation diagram indicates overall modulation health.

Our ATM interface connects to a 155 Mb/s optical fiber and extracts MPEG transport streams from several VP/VCs (virtual path/virtual circuit). In addition to this basic functionality, the interface detects physical layer errors and parameters with the optical and Sonet/SDH signals.

For More Information

To learn more about the DVStation, request a demo, or learn how Pixelmetrix might help you optimize video network integrity, contact us today!

On the Internet: sales@pixelmetrix.com
www.pixelmetrix.com

North America: 1-877-71-PIXEL
Europe: +41-79742-7454
Asia Pacific: +65-547-4935

About the Author

Harshang Pandya is a Senior Design Engineer with Pixelmetrix Corporation, manufacturer of the DVStation, a preventative monitoring solution for digital broadcast networks.